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HIGHLY STABILIZED, ULTRA-LOW NOISE FET OSCILLATOR WITH DIELECTRIC RESONATOR

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Abstract

A highly stabilized ultra-low noise GaAs FET oscillator, using a temperature stabilized dielectric resonator in the feedback circuit, has been developed. A key factor for achieving high stability and low noise is a very high loaded Q (8000).

The oscillator operates at 4 GHz with a power output of 11.5 dBm, a frequency temperature coefficient of $\pm$0.02 ppm/^{o}C, and a SSB N/C ratio of -130 dBc/Hz and -146 dBc/Hz at 10 KHz and 100 KHz off carrier, respectively. The oscillator is varactor tunable over a 1500 KHz bandwidth.

Introduction

The oscillator we developed is a VCO to be used in a carrier recovery phase-locked loop for a Coherent Quadrature Phase-Shift-Keyed (CQPSK) demodulator. A small degree of electronic tuning is required to track variations of the center frequency of the CQPSK signal as well as any long term drift of the oscillator.

This paper describes a high stability GaAs FET oscillator that includes a high gain amplifier connected in a feedback loop with a temperature stabilized very high Q dielectric resonator in an invar cavity. Experimental results showed that the VCO has both excellent frequency stability versus temperature and very low phase noise.

Oscillator Design

The block diagram of the dielectric resonator oscillator (DRO) is shown in Fig. 1. The active component is a temperature compensated miniature two-stage FET amplifier operating at 4 GHz with a gain of 20 dB. The signal from the amplifier is divided by a lumped-element quadrature coupler. The amplifier and the coupler were fabricated using the miniature ceramic circuit (MCC) technology reported earlier [1]. One port of the coupler supplies the output signal, while the other port feeds the signal to a lightly coupled dielectric resonator filter. The light coupling allows us to achieve a loaded Q which is only 5% below the unloaded Q of the resonator. The insertion loss of the filter is 12 dB, which is compensated by 16 dB amplification - including the loss of the output power splitter - leaving an excess loop gain of 4 dB.

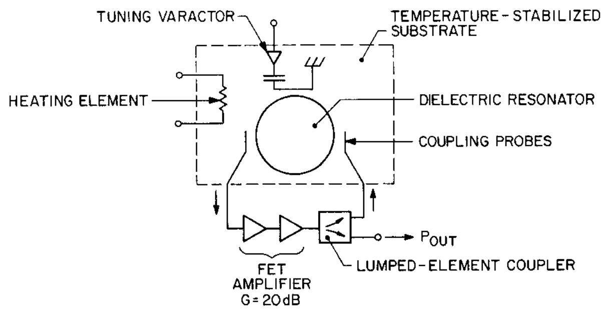

Fig. 1. Block Diagram of Dielectric Resonator Oscillator

A photograph of the dielectric resonator oscillator is shown in Fig. 2. The cylindrical cavity, made out of invar, contains a $ZrSnTiO_3$ dielectric resonator, mounted in the center of the cylinder. The use of a large metal cavity to shield the dielectric resonator is considered important since experiments indicated that the Q of the dielectric resonator is drastically affected by the proximity of metal walls. The resonator, mounted on a ceramic substrate supported by quartz spacers, is kept at a constant temperature (+55 $\pm$ 0.5^{o}C) by a controller and a small heating resistor mounted on the substrate. The rectangular case, also shown in Fig. 2, includes the 20 dB amplifier and the 3 dB output power splitter.

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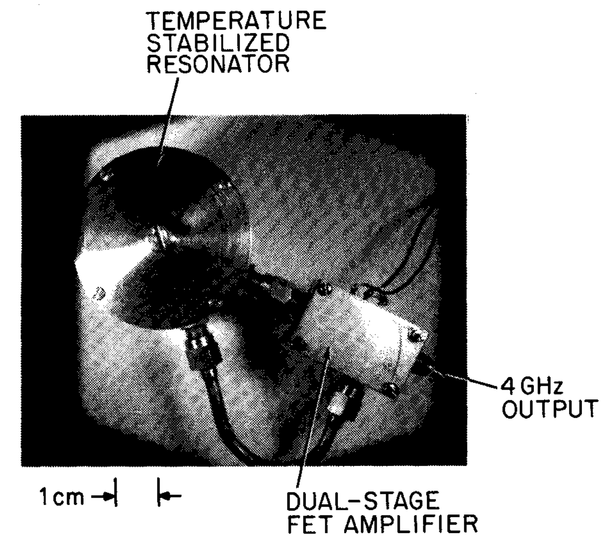

Fig. 2. Photograph of Dielectric Resonator Oscillator

Experimental Performance

Table I summarizes the performance of the oscillator. Fig. 3 shows the output power and frequency deviation of the oscillator as a function of the ambient temperature. The total frequency drift is only ±4 KHz (±1 PPM) when the ambient temperature varies from 0^oC to 50^oC. This corresponds to a frequency stability temperature coefficient of ±0.02 PPM/^oC. Fig. 4 illustrates the electronic tuning characteristic of the oscillator. A 1500 KHz tuning range was achieved without significant variation in output power, efficiency, or phase noise.

The spectral density of the oscillator phase noise, measured using the HP 11729B/8566A noise test system, is shown in Fig. 5. The SSB N/C ratio is -130 dBc/Hz and -146 dBc/Hz at frequencies 10 KHz and 100 KHz off carrier, respectively. These results, as well as other results obtained from other commercial units or derived from published data, are listed in Table II. For a meaningful comparison, the FM noise of oscillators operating at frequencies other than 4 GHz, was scaled by a factor of -20 log ($f_o/4x10^9$), where f_o is the operating frequency of oscillator under test. It is believed that our phase noise results are the best reported for free running GaAs FET oscillators at this frequency. This excellent noise performance is attributed to the very high loaded Q of the oscillator afforded by the high gain of the amplifier and by the high Q of the dielectric resonator suspended in the large cavity. Fig. 6 shows output power, drain bias pushing and efficiency of the oscillator. Linear variation of output power with drain bias allows convenient control of the power with small frequency variations. The drain voltage pushing figure is less than 20 KHz/V at 4 V. Output power, frequency deviation, and efficiency of the DRO as a function of gate bias voltage is shown in Fig. 7. A linear tuning of 280 KHz can be achieved with a power variation of less than 0.4 dB. This gate bias tuning is used for a 2nd order frequency-temperature compensation. Mechanical tuning of the oscillator, implemented with a tuning screw in the metal cavity, resulted in frequency tuning of 2 MHz for a power variation of less than 0.2 dB.

TABLE 1 — Performances of the Dielectric Resonator Oscillator

Oscillation Frequency	4.000 GHz
Output Power	11.5 dBm
Efficiency	6%
Electronic Tuning Range	1500 kHz
Loaded Q	8000
Frequency Stability	±4 kHz (0°C ~50°C)
Phase Noise	−130 dBc/Hz at 10 kHz off carrier
	−146 dBc/Hz at 100 kHz off carrier
Spurious Output	Harmonics <−30 dBc
	Nonharmonics<−80 dBc

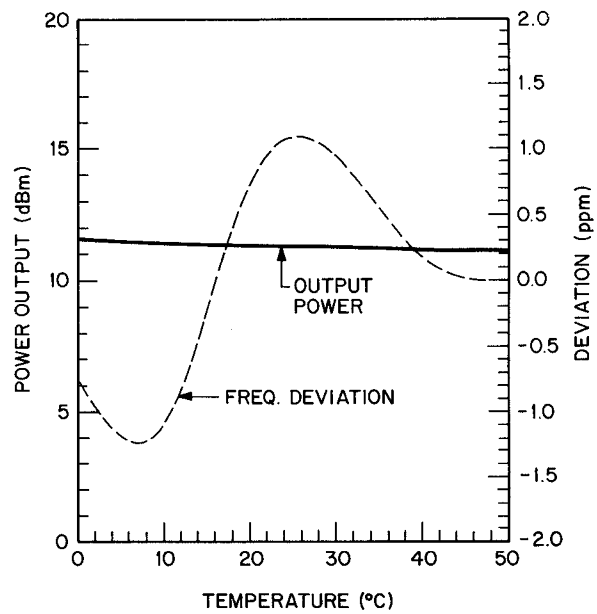

Fig. 3. Output Power and Frequency Deviation of DRO as a Function of Ambient Temperature

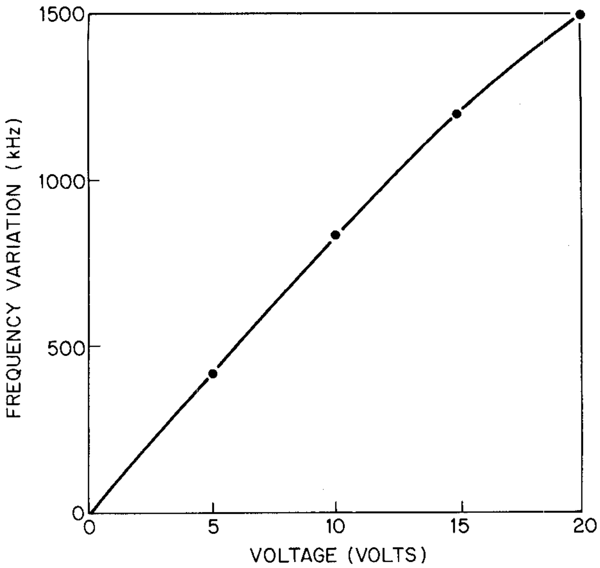

Fig. 4. Tuning Characteristic of DRO

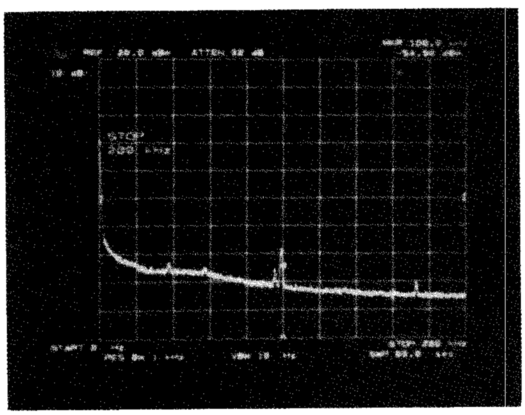

Fig. 5. Photograph of Phase Noise Performance

TABLE 2 — COMPARISON OF PHASE NOISE CHARACTERISTICS

	Phase Noise (dBc/Hz)	
	10 kHz	100 kHz
FET DRO (this work) 4 GHz	−130	−146
Klystron Oscillator[2] (HP) 4 GHz	−90	−101
*FET DRO[3] (Frequency Source, Inc.) 17 GHz	−111	−132
Crystal Oscillator[4] (Frequency Source, Inc.) 4 GHz	−107	−114
*FET DRO[5] (M. Camiade) 11 GHz	−113	−143
*FET DRO[6] (O. Ishihara) 11 GHz	−99	−135
*FET DRO[7] (C. Tsironis) 11 GHz	−78	−118
*FET DRO[8] (H. Abe) 6 GHz	−90	−113
*Unstabilized FET Oscillator[8] (H. Abe) 6 GHz	−53	−80

*Phase noise scaled to 4 GHz.

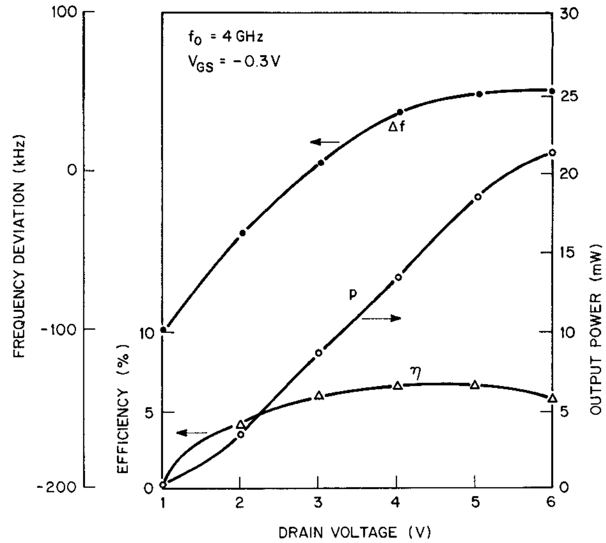

Fig. 6. Output Power, Frequency Deviation, and Efficiency of DRO as a Function of Drain Bias

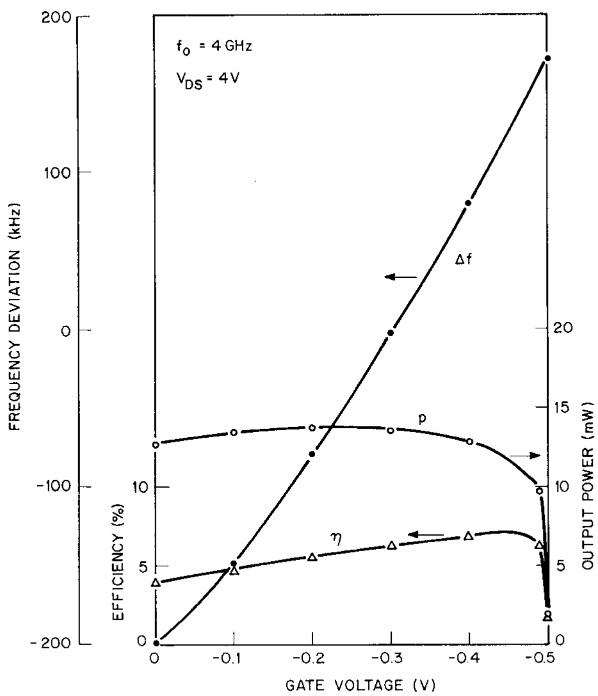

Fig. 7. Output Power, Frequency Deviation, and Efficiency of DRO as a Function of Gate Bias

Conclusion

The GaAs FET oscillator, with a temperature-stabilized very high loaded Q dielectric resonator in a high gain feedback circuit, performed with excellent frequency stability and phase noise. These phase noise results set the state of the art for FET oscillators. The oscillator provided an output power of 11.5 dBm at 4 GHz with a frequency temperature coefficient as low as ± 0.02 PPM/^{o}C. Phase noise level was -130 dBc/Hz and -146 dBc/Hz at 10 KHz and 100 KHz off carrier, respectively. A 1500 KHz electronic tuning was achieved without significant variation in output power, efficiency or the phase noise.

References

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